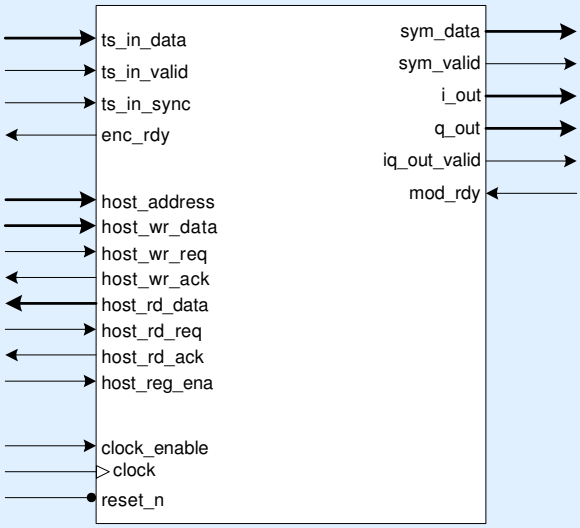
J.83abc/DVB-C Cable FEC Encoder

CMS0017

- Provides the required channel encoding functions for cable television as specified by ITU Recommendation J.83 Annexes ABC and DVB-C.
- Standard 188-byte MPEG Transport Stream input.
- Mapped I-Q and unmapped symbol data outputs are both available
- C / C++ header file defines Host Interface registers, allowing software mode control.
- External RAM interface for long interleave modes.
- Synthesis control to build for any subset of the supported modes, removing unneeded logic.



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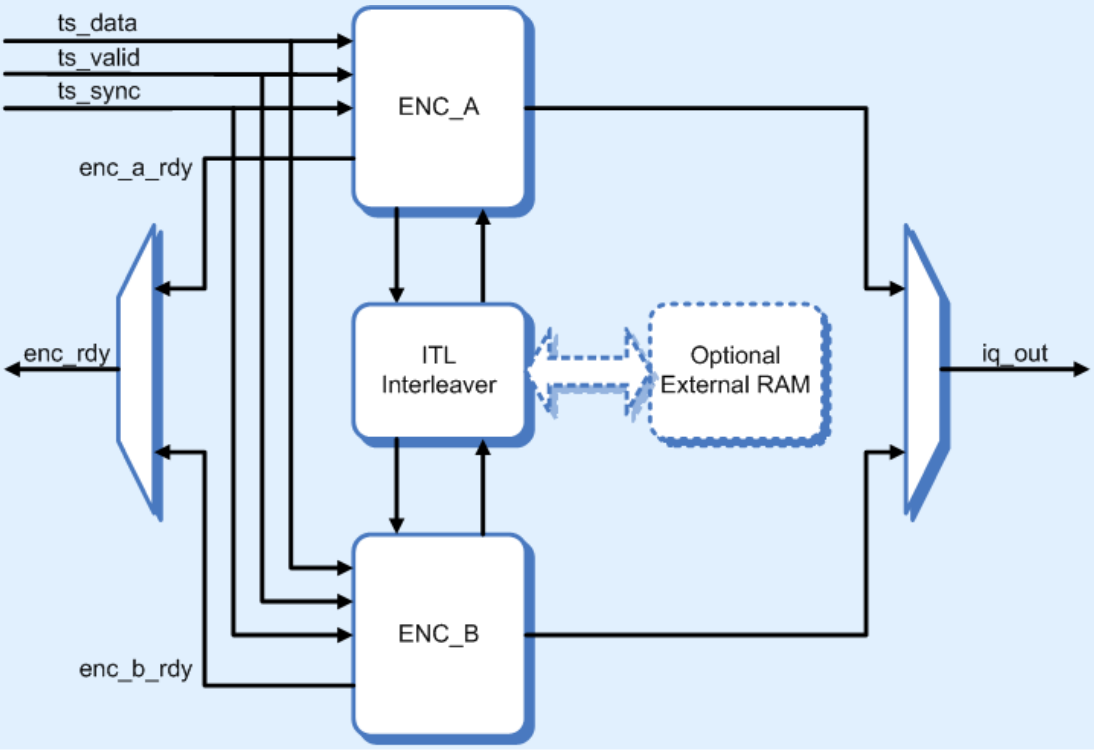
Block Diagram



Detailed Description

The Commsonic CMS0017 J.83abc/DVB-C Cable FEC Encoder combines all of the channel coding and Forward Error Correction functions specified by DVB-C and by J83 - Annexes A B and C. However, it does not include the Root-Raised-Cosine filters required by these standards.

The CMS0017 includes functions for framing, scrambling, interleaving, Reed-Solomon coding, trellis coding, and QAM mapping.

With the exception of the common interleaver block, two independent datapaths are required. J83A J83C and DVB-C are quite similar in requirements. These are implemented in the ENC_A sub-block

The requirements of J83 Annex B are significantly different. The largest difference is the addition of trellis encoding, but the Reed-Solomon code is also uniquely different and the scrambler is based on a different algorithm.

In practice, only the interleave block may be easily shared between them.

ENC_A (DVB-C and J.83 Annex A + C)

The ENC_A sub-block supports the full set of DVBC constellations, of which J.83 Annex A and C are subsets. This includes 16-, 32-, 64-, 128- and 256-QAM.

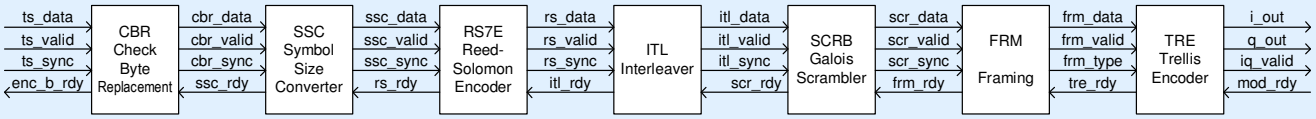
These modes use a single interleave configuration.

Mode control is provided via the host interface registers. Annex A/C-mode is selected by setting the ***AnnexBEnable*** register = 0.

The number of bits per symbol is set by ***QamMode*** = bits_per_symbol – 4

Detailed Description (Cont'd)

ENC_B (J.83 Annex B)



The ENC_B sub-block supports J.83 Annex B.

CBR replaces the 0x47 MPEG sync byte with a checksum, used in the decoder both as a method of sync detection and to monitor the decoded transport stream for errors.

SSC converts the 8-bit Transport Stream bytes into 7-bit data symbols for the Reed-Solomon Encoder. The 7-bit RS(128,122) code contains one extension symbol.

The Interleaver supports the full set of J.83 B modes, but there is a synthesis option for the short (128x1) modes specified for DOCSIS 1.0 and 1.1, reducing memery requirements by a factor of eight.

The scrambler is based on a second-order Galois polynomial using the same 7-bit Galois Field as the Reed-Solomon Encoder.

The Framer block synchronises the Scrambler and the Trellis Encoder to the RS packet boundaries. A fixed sync pattern is followed by a four-bit field specifying the Interleave mode to be used by the decoder.

Mode control is provided via the host interface registers. Annex B mode is selected by setting the ***AnnexBEnable*** register = 1.

The number of bits per symbol is set by ***QamMode*** = bits_per_symbol – 4.

The 4-bit ***ItlMode*** is encoded as specified in J.83 Annex B.

Synthesis Parameters

Build parameters are defined in a VHDL package and applied to the design as GENERICs.

These are fixed at synthesis time.

Name	Description	Default
build_soft_reset	Selects whether to build a software reset under host control	TRUE
build_clock_enable	Selects whether to build the clock_enable logic	TRUE
build_mapper	In many applications, scaled IQ mapping is performed in the QAM modulation block. Set build_mapper = FALSE if the CMS0017 IQ outputs are unused.	TRUE
build_external_itl_ram	Selects whether to build the external RAM interface (TRUE) or instantiate internal RAM (FALSE).	FALSE
itl_read_delay	Specifies the number of clock cycles from valid itl_ram_addr until itl_rd_data is latched internally. Default value for local synchronous ram is 2	2
build_j83_a	Selects whether to build support for J.83 Annex A	TRUE
build_j83_b	Selects whether to build support for J.83 Annex B	TRUE
build_j83_c	Selects whether to build support for J.83 Annex C	TRUE
build_dvb_c	Selects whether to build support for DVB-C	TRUE
build_docsis_itl	If true, only the shorter Annex B interleave modes are built in accordance with DOCSIS 1.0 and 1.1. Note that DOCSIS 2.0 and 3.0 specify the full range of Annex B modes.	FALSE
host_addr_width	Width of the host address bus	8
host_data_width	Width of the host data bus	8

Principle I/O Description

Host Interface	
host_addr	8-bit register address
host_reg_ena	Active high enable (chip select) Must be high for read or write access.
host_wr_data	8-bit RAM write data
host_wr_req	1 => write cycle request (write data valid)
host_wr_ack	1 => write cycle acknowledge. Because there is no internal arbitration for RAM, CMS0017 always accepts write data and this output is always true.
host_rd_data	8-bit RAM read data
host_rd_req	1 => read cycle request. Must be held high until host_rd_ack = 1.
host_rd_ack	1 => read cycle acknowledge (read data valid). This signal indicates that read data is valid. Goes high one cycle after host_rd_req.
Encoder I/O	
ts_in_data	Uncoded data input bytes
ts_in_valid	1 => uncoded data and sync inputs are valid
ts_in_sync	1 => current input byte is first in TS packet (0x47)
enc_rdy	1 => Encoder ready for new data byte. Data transfer occurs when enc_rdy = ts_in_valid = 1
sym_data	The encoded data output symbols (unmapped)
sym_valid	Indicates current output symbol is valid when unmapped output is selected.
i_out	This 5-bit signed output represents the in-phase portion of the mapped symbol
q_out	This 5-bit signed output represents the quadrature portion of the mapped symbol
iq_out_valid	Indicates current output symbol is valid when mapped output is selected.
mod_rdy	Interface ready for new data byte. Data transfers when mod_rdy = sym_valid (= iq_valid) = 1
External Memory Interface	
itl_ram_addr	16-bit ram address
itl_wr_ena	Active high RAM write enable
itl_wr_data	8-bit RAM write data
itl_rd_data	8-bit RAM read data
Others	
clock	Clock Input.
reset_n	Asynchronous reset input (active low).
clock_enable	This is actually a logic enable. Logic results are captured on the rising clock edge when clock_enable = 1.

Host Interface

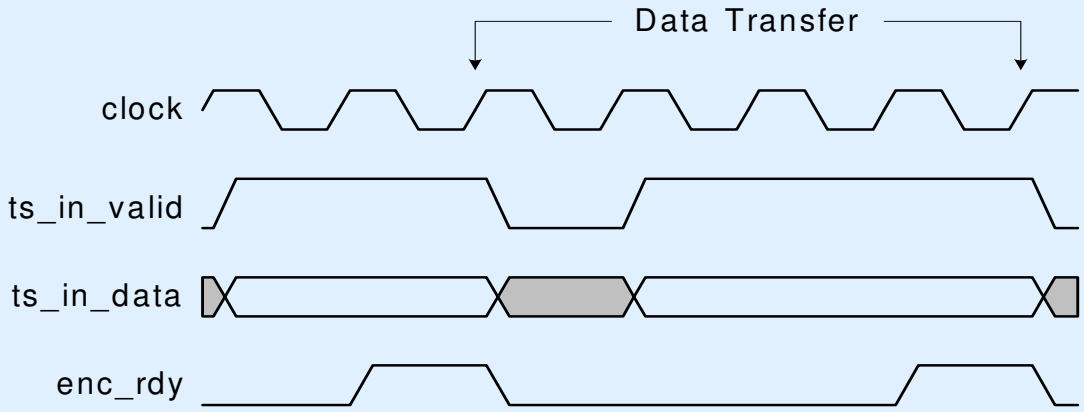
The host interface registers allow software to control the encoder's mode of operation. For programming convenience, the CMS0017 package includes a standard C / C++ header file defining the host register bank as a structure. The members of that structure are as follows:

Name	Address	Description
SoftReset	0x00	Write 1 to this register to force all internal states to reset. Remaining register contents are unaffected. This register dafults to 1 on hardware reset, so a zero must be written here to enable the core.
Version	0x04	This read-only register returns the version number of the core.
AnnexBEnable	0x08	1 => Annex B mode. 0 => Annex A+C+DVBC
QamMode	0x0C	Specifies the number of bits per symbol : QamMode = bits_per_symbol – 4
ItlMode	0x10	When in Annex B mode, this register specifies the Interleave mode. Encoding matches that of J.83 Annex B :

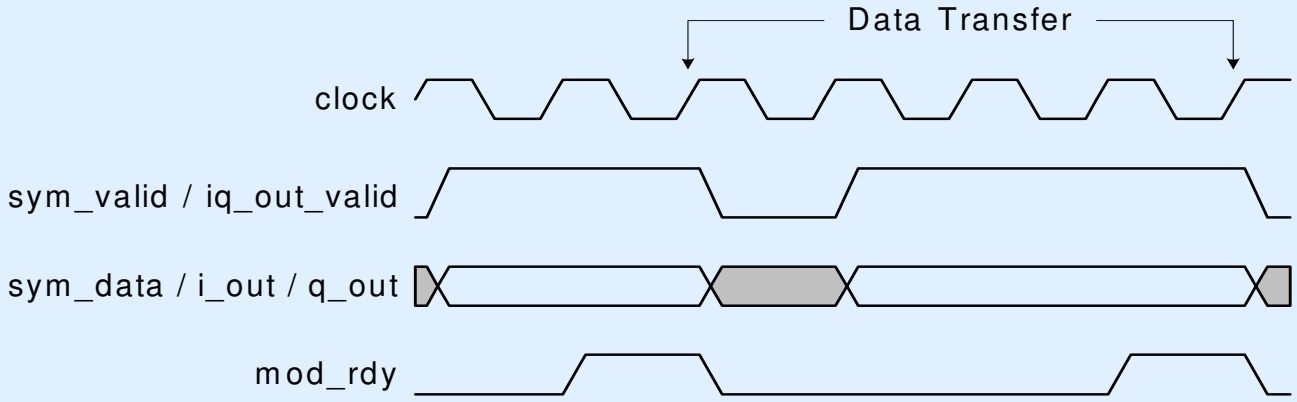
Timing Diagrams

The input and output data interfaces are implemented with RDY-VALID handshaking. This provides a simple interface in which each block may moderate the data flow to match its own data processing requirements. The data source asserts its VALID flag when it presents data. The data destination indicates availability using its RDY flag. Data transfer occurs synchronously when both the source's VALID and the destination's RDY = 1.

Transport Stream Input:



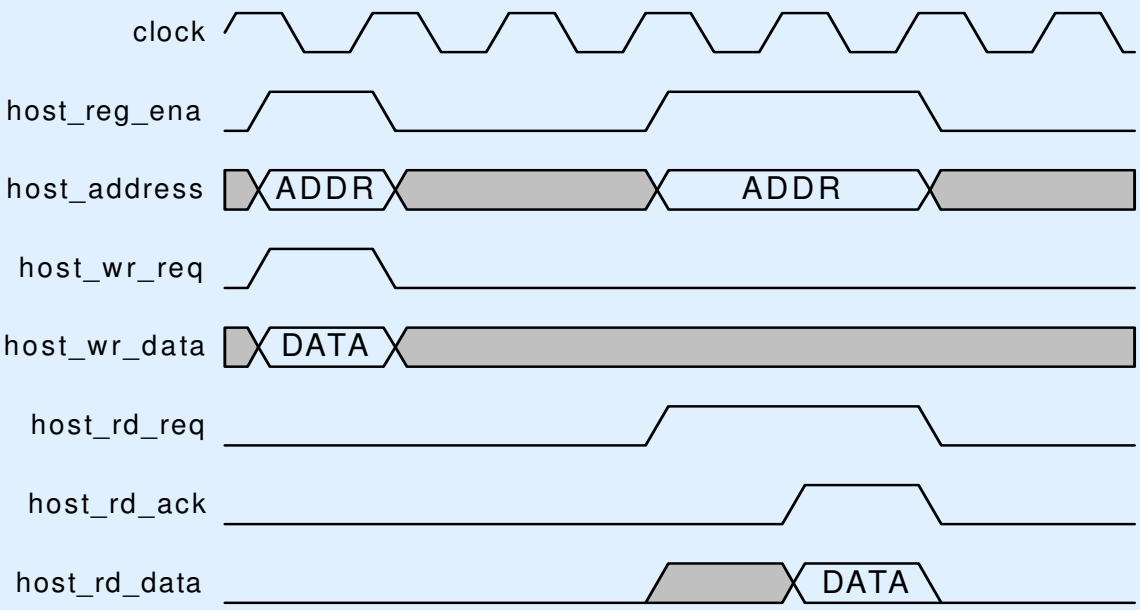
Symbol Output:



Timing Diagrams (Cont'd)

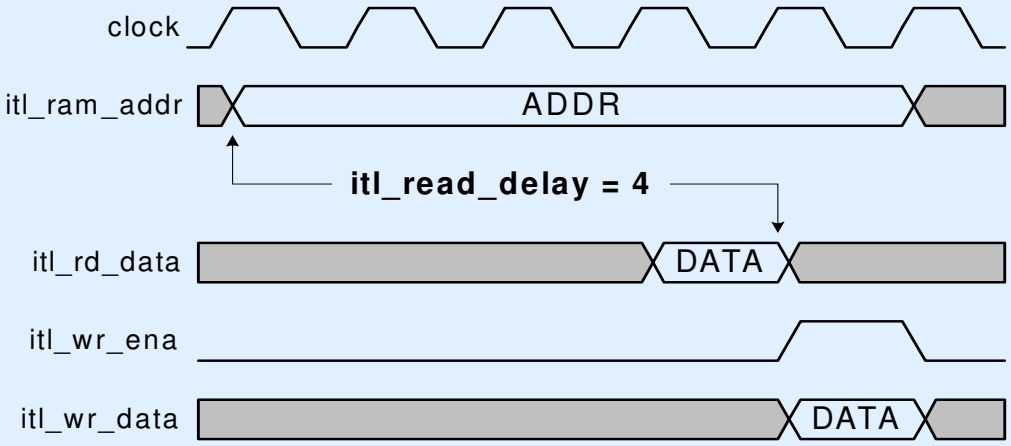
Host Interface:

The Host Interface is synchronous with the system clock input. The REQ - ACK handshake is similar to the RDY-VALID handshake used for the data interfaces.



External Memory Interface:

The CMS0017 may be configured to use memory external to the core. The timing of this interface is controlled by the synthesis constant **`itl_read_delay`**, illustrated below.



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S2, DVB-C/J.83/A/B/C and DVB-T/H.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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